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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,387	11/25/2003	Manabu Minowa	OKI.598	4269

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EXAMINER	
AMAYA, CARLOS DAVID	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 05/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,387	MINOWA, MANABU	
	Examiner	Art Unit	
	Carlos Amaya	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 2 and 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura (JP 06042575) in view of Kimura (US 5,016,223).

With respect to claim 1 Nakamura in view of Kimura discloses an interface circuit for inputting/outputting a signal between first and second apparatuses (Circuit 1 and Circuit 2 Figure 1) having different power units (Power source 3 and 4), respectively, comprising: a power node to which a first power voltage that is supplied from the power unit of said first apparatus is outputted (Power node being the point at which the Power

source 3 is connected to Circuit 1); a 3-state buffer (3 State buffer 6) which is driven by a second power voltage that is supplied from the power unit of said second apparatus (As shown in figure 1 buffer 6 is driven power source 4 of second apparatus) and in which the output of the signal that is supplied from said second apparatus is controlled by an electric potential at said power node (Figure 1 shows buffer 6 receiving a control signal from the second.apparatus ; also the buffer receives a Vdd electric potential as shown in circuit 1 from the electrical node).

Nakamura, however, does not disclose an analog switch which is driven by said second power voltage and in which a connection between an output side of said 3- state buffer and a logic circuit in said first apparatus is controlled by the electric potential at said power node.

Kimura discloses a memory card circuit with a 3 state buffer (34,35) and analog switch 30 shown in figure 5 (a), the analog switch 30 is for controlling a signal (Kimura's invention is being used only to show that analog switches are used to control signals).

It would have been obvious at the time the invention was made to have included Kimura's analog switch in Nakamura's invention.

The suggestion or motivation for doing so would have been to provide an analog switch, which depending upon a received signal control its operation it turns on/off preventing/allowing power/signal to flow.

With respect to claim 2 Nakamura in view of Kimura discloses an interface circuit for inputting/outputting a signal between first and second apparatuses (Circuit 1 and Circuit 2 Figure 1) having different power units (Power source 3 and 4), respectively,

comprising: a power node to which a first power voltage that is supplied from the power unit of said first apparatus is outputted (Power node being the point at which the Power source 3 is connected to Circuit 1); a voltage detector which detects a voltage at said power node and outputs a control signal when said voltage exceeds a reference voltage (Sag detectors in figures 1-3, which detects a predetermined potential difference in the supply voltage, Paragraph 0018, lines 12-14); a 3-state buffer (3 State buffer 6) which is driven by a second power voltage that is supplied from the power unit of said second apparatus (As shown in figure 1 buffer 6 is driven power source 4 of second apparatus) and in which the output of the signal that is supplied from said second apparatus is controlled by an electric potential at said power node (Figure 1 shows buffer 6 receiving a control signal from the second apparatus ; also the buffer receives a Vdd electric potential as shown in circuit 1 from the electrical node).

Nakamura, however, does not disclose an analog switch, which is driven by, said second power voltage and in which a connection between an output side of said 3- state buffer and a logic circuit in said first apparatus is controlled by said control signal.

It would have been obvious at the time the invention was made to have included Kimura's analog switch in Nakamura's invention.

The suggestion or motivation for doing so would have been to provide an analog switch, which depending upon a received signal control its operation it turns on/off preventing/allowing power/signal to flow.

With respect to claim 3 Nakamura in view of Kimura discloses 3. An interface circuit for inputting/outputting a signal between first and second apparatuses having

different power units, respectively, comprising: a power node to which a first power voltage that is supplied from the power unit of said first apparatus is outputted (Power node being the point at which the Power source 3 is connected to Circuit 1, Vdd); a voltage detector which outputs a control signal when a voltage at said power node exceeds a reference voltage (Sag detectors in figures 1-3, which detects a predetermined potential difference in the supply voltage, Paragraph 0018, lines 12-14, depending on the sense change in the supply voltage a control signal is emitted to the buffers. Power node being voltage at Vdd being supply to the sag detector); a 3-state buffer which is driven by a second power voltage that is supplied from the power unit of said second apparatus (As shown in figure 1 buffer 6 is driven power source 4 of second apparatus), controls the signal that is supplied from said second apparatus in accordance with a voltage that is applied to a control terminal and supplies said signal to a logic circuit in said first circuit (Output of buffer 6 in circuit 1 is outputted to the circuit 2 to cease operation of the receiving circuit 2).

Nakamura, however, does not disclose an analog switch that is driven by said second power voltage and in which a connection between said power node and the control terminal of said 3-state buffer is controlled by said control signal.

It would have been obvious to a person of ordinary skill in the art at time the invention was made to connect an analog switch as disclosed by Kimura, in Nakamura's invention and, which is controlled by the control signal generated by the voltage detector.

The suggestion or motivation for doing so would have been to provide an analog switch, which depending upon a received signal control its operation it turns on/off preventing/allowing power/signal to flow.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to the examiner's supervisor, Brian Sircus who can be reached on (571)272-2800. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CA

PHUONG T. VU
PRIMARY EXAMINER